AMENDMENTS TO THE CLAIMS

Please amend the claims as shown below:

Claim 1 (Currently Amended). A DC-DC converter that converts a first DC voltage to a second DC voltage comprising:

a first output configured to control a first switch ~~connected~~ coupled to an input of the first DC voltage;

a second output configured to control a second switch, wherein the first and second switches are controlled by respective first and second input signals to generate the second DC voltage;

a sensing device configured to receive a sense ~~signal~~ current representative of a current through ~~one of~~ the ~~first or~~ second ~~switches~~ switch and responsively form a first current and a second current that are representative of the current through the second switch; and

a control circuit configured to receive the first current and the second current and ~~to~~ selectively control ~~at least one of~~ a first delay time between ~~disabling the first switch and enabling the second switch or a second delay time between~~ disabling the second switch and enabling the first switch ~~responsively to the sense signal~~, the control circuit also configured to use the first current to selectively decouple the sense current from the control circuit.

Claim 2 (Currently Amended). The DC-DC converter of claim 1, wherein the control circuit includes a delay circuit and wherein the control circuit is configured to receive a PWM input and delay the first delay time before forming an active state of the first input signal and wherein the control circuit is configured to receive the PWM input and

delay ~~the~~ a second delay time before forming an active state of the second input signal.

Claim 3 (Original). The DC-DC converter of claim 2, wherein the delay circuit comprises a charge controlled delay circuit.

Claim 4 (Original). The DC-DC converter of claim 2, wherein the delay circuit comprises a digital controlled delay circuit.

Claim 5 (Currently Amended). The DC-DC converter of claim 1, wherein the sensing device is configured to receive the sense ~~signal~~ current and responsively form ~~a~~ the first current ~~sense signal~~ that is representative of a conduction current through the second switch and form ~~a~~ the second current ~~sense signal~~ that is representative of a current through a body diode of the second switch ~~wherein the first and second current sense signals are representative of the sense signal and wherein~~ , the sensing device ~~is~~ configured to store a value of the first current ~~sense signal~~ as a first stored value and store both a value of the second current as a second stored value during at least a portion of an active time of the second input signal, and to compare the first stored value to a value of the second current ~~sense signal~~ to determine the ~~second~~ first delay time.

Claim 6 (Original). The DC-DC converter of claim 1, wherein the second switch comprises a power MOSFET device.

Claim 7 (Previously Presented). The DC-DC converter of claim 6, wherein the sensing device senses current conduction of a body diode of the second switch.

Claim 8 (Currently Amended). A synchronous DC-DC converter structure comprising:

a high-side MOSFET switch having a drain coupled to an input DC voltage and a source coupled to a switch node;

a low-side MOSFET switch having a drain coupled to the switch node and a drain coupled to a ground node;

a sensing ~~device~~ transistor having a drain coupled to the switch node for selectively forming a sense current ~~sense signal~~ that is representative of current in the low side MOSFET switch; and

a control structure configured to receive the sense current and responsively form a first current that is representative of the current in the low side MOSFET switch and a second current that is representative of the current in the low side MOSFET switch, the control structure configured to store the first current as a first value and store the second current as a second value during a portion of an active time of the low side MOSFET switch and to disable storing the first value prior to disabling the low side MOSFET switch, the control structure configured to selectively adjust a delay time between turning off ~~one of the high-side MOSFET switch and~~ the low-side MOSFET switch and turning on ~~the other of~~ the high-side MOSFET switch ~~and the low-side MOSFET switch~~ and configured to use the first current and the second current to selectively form the sense current.

Claim 9 (Currently Amended). The structure of claim 8, wherein the control structure is coupled to an adjustable delay circuit ~~and wherein the control structure is configured to form a first current sense signal and a second current sense signal that are representative of the current sense signal and wherein the control circuit is further configured to store a value of the first current sense~~

~~signal and compare the stored value to a value of the second current sense signal to selectively adjust the delay time~~.

Claim 10 (Previously Presented). The structure of claim 9 wherein the adjustable delay circuit comprises a digital controlled delay circuit.

Claim 11 (Previously Presented). The structure of claim 9 wherein the delay circuit comprises a charge controlled delay circuit.

Claim 12 (Currently Amended). The structure of claim 8, wherein the sensing ~~device~~ transistor comprises a MOSFET ~~device~~transistor .

Claim 13 (Currently Amended). The structure of claim 8, wherein the sensing ~~device~~ transistor senses body diode current conduction in the low-side MOSFET switch.

Claim 14 (Currently Amended). The structure of claim 8, wherein the sensing ~~device~~ transistor senses cross conduction current in the low-side MOSFET switch.

Claim 15 (Currently Amended). A method for controlling delay time in a synchronous DC-DC converter having a high-side switch coupled to a low-side switch comprising the steps of:

selectively forming a ~~first current~~ current sense signal representative of a current in the low-side switch; ~~and~~

using the current sense signal to form a first current and a second current that are representative of the current sense signal;

storing a value of the first current as a first stored value and storing a value of the second current as a second

stored value during at least a portion of an active time of the low-side switch;

disabling storing of the first current while holding the first stored value and maintaining storing the second current as the second stored value prior to disabling the low-side switch;

selectively controlling a delay time between turning off ~~one of the high-side switch and~~ the low-side switch and turning on the ~~other of the~~ high-side switch ~~and the low-side switch~~ responsively to the ~~current sense signal~~first stored value and the second stored value; and

using the first stored value and the second stored value for selectively forming the current sense signal.

Claim 16 (Previously Presented). The method of claim 15 wherein the step of selectively controlling the delay time includes increasing the delay time.

Claim 17 (Previously Presented). The method of claim 15 wherein the step of selectively controlling the delay time includes decreasing the delay time.

Claim 18 (Currently Amended). The method of claim 15 wherein the step of selectively forming the ~~first~~ current sense signal includes sensing current in the low-side switch with a MOSFET ~~device, forming a first current sense signal and a second current sense signal that are representative of the first current, storing a value of the first current sense signal, and comparing the stored value and the second current sense signal~~ and wherein the step of using the first stored value and the second stored value for selectively forming the current sense signal includes using the first stored value and the second stored value for disabling the MOSFET.

Claim 19 (Currently Amended). The method of claim 15, wherein the step of selectively controlling the delay time includes controlling the delay time with a digital controlled delay circuit.

Claim 20 (Currently Amended). The method of claim 15, wherein the step of selectively controlling the delay time includes controlling the delay time with a charge controlled delay circuit.